Current Sensor for the Silicon Strip Detector's at BRAHMS

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Abstract

Accurate and reliable measurement of the bias current for the Silicon Strip Detector's is not currently possible using the LeCroy 1461M/410 power supply's current readout. We have designed a current sensor which would be put in series with the LeCroy power supplies and the Silicon Strip Detectors to provide a reliable and accurate measurement of the Silicon Strip Detector bias current.

The Problem

Passage of charged particles through a Silicon Strip Detector can degrade the Silicon Strip Detector, resulting in increasing bias current over time. This bias current creates a voltage drop across the 40MΩ biasing resistors, thereby reducing the voltage supplied to bias the Silicon Strip Detectors by our LeCroy 1461M/410 power supplies. In order to know the detectors are appropriately biased, we must therefore have an accurate measurement of this bias current. Our LeCroy 1461M/410 power supplies can supply a maximum of 120V. So, if one of the Silicon Strip Detectors were to breakdown completely, we could expect a maximum current of 3μA=120V/40MΩ.

The specifications sheet for the LeCroy 1461M/410 power supply quotes a resolution (the minimum change in current output measurable by the readout) of 26nA and an accuracy of ±(1% of reading + 500nA). In other words, regardless of the current being supplied, the supply's measurement can be no more accurate than .5μA, or ~17% of our maximum bias current. This is clearly not sufficient to measure typical bias currents.

Furthermore, we see fluctuations in the current reading over short periods of time of ~200nA. This is a factor of 10 greater than the specifications 26nA, and may indicate a problem with the supplies. This should be investigated.

The Solution

We have developed a working prototype of a current sensor which would be placed in series with the power supply and the Silicon Strip Detector pre-amp shaper board. As low-side (between the detector and ground) sensing is not possible, we are forced to implement a high-side (between the power supply and detector) current sensor. Because we require a high input impedance and have to accommodate a high-common mode voltage, a non-trivial design is required.

The prototype sensor schematic (3 pg) and single channel layout (1 pg) are available in .pdf.

In short:

> The sensor circuit consists of a "floating" (isolated from the system ground) sense circuit using an instrumentation amplifier (INA116 Instrumentation Amplifier - U1/INA116/SO - top middle, pg 1)) for sensing the bias current and an optical isolation amplifier (HCPL7800 Optical Isolation Amplifier - U2/HCPL7800 - top right, pg 1) to bridge the isolation boundary to the power-supply ground referenced circuitry (TLE2082 High-Speed, Dual JFET-Input Operational Amplifier - U3/TLE2081/SO - middle middle, pg 2) whose first amplifier provides additional amplification and differential to single-ended conversion for the (HCPL7800, and whose second amplifier supplies output drive for the 50Ω input impedance of a FERA and corrects the inherent offset in the other components in the signal path into the 0V to -1V range required by the FERA. The remaining circuitry is to provide for power decoupling, ground isolation, and supply voltage regulation.

In detail, the sensor has three aspects:

1. Signal:
   The detector bias current flows in through the board-edge SMA connector (J5/CON3 - top left, pg 1 - this is the power-

supply side connection), through the 10KΩ sense resistor, and out through the board-edge SMA connector (J6/CON3 - top left, pg 1 - this is the detector side connection). The shields of the SMAs are not connected to the floating ground. The bias current is measured and amplified by the INA116 Instrumentation Amplifier (U1/INA116/SO - top middle, pg 1) and is programmed for a gain of ~6.77 V/V by the 8.66K resistor (R6 - top). The ultra-high input impedance and ultra-low input bias current of the INA116 result in a negligible measurement error being introduced.
To address the high common mode voltage, the output of the INA116 is applied to the input of an HCPL7800 Optical Isolation Amplifier (U2/HCPL7800 - top right, pg 1) which consists of a sigma-delta analog-to-digital converter (ADC), a serial digital optical communications link across the isolation boundary (provided by the NTA0512), and a digital-to-analog converter (DAC) to provide a differential analog output voltage biased about +2.5V and a gain of ~8.0 V/V.

> Note: The input (left-hand) side of the HCPL7800 is powered and grounded by elements on the "floating" ground, while its output (right-hand) side is powered and grounded by the power-supply.

On the power-supply side of the isolation boundary, the TLE2082 High-Speed, Dual JFET-Input Operational Amplifier's (U3/TLE2082/SO - middle middle, pg 2) first stage is configured as a difference amplifier with a gain of ~-1.10 V/V. This converts the differential output of the (HCPL7800 to a single-ended signal. A reference diode (D1/1NA4733A - upper middle, pg 2) is used to provide a stable +2.5V reference for the second amplifier of the which is used to provide offset correction and sufficient current to drive the 50Ω input impedance of the FERA. This second amplifier can be configured (using R35, R36 and R38) to shift the offset due to the rest of the signal path either in the negative or positive direction.

> Note: The overall offset of the signal path is a function the offsets inherent in the individual components, and cannot be accurately predicted. Components from the same manufacturer batch are likely to have very similar offsets (and other characteristics), but it may be necessary to populate each channel entirely except for R35, R36 and R38, measure the offset, and select these components to shift the overall offset into the FERA's -1V - 0V input range.

Overall, the gain from the sense resistor to the output is .67 V/µA, providing a -2V output for a 3µA detector bias current. When connected to the FERA, the 50Ω resistor forms a divider thus yielding a 0V to -1V signal for the 0µA to 3µA bias current range. The output of the sensor is taken off by a board-edge SMA connector (J7/CON3 - middle right, pg 2).

2. Grounding:
   The ground planes of the sensor are AC coupled (C24 & C25 - bottom middle, pg 3) in order to eliminate switching noise from the NTA0512 DC-DC Converter (UF/NTA0512M - top middle, pg 3), which was observed on the output of the INA116 (U1/INA116/SO - top middle, pg 1). The power supply common needs to be tied to earth ground or the floating ground portion of the sensor will pick up 60Hz noise.

3. Power:
   Regulated ±5V power is brought to the board from an external power supply through a four-lead board connector (J4/CON4 - top left, pg 3) and is decoupled. The NTA0512 (UF/NTA0512M - top middle, pg 3) provides an unregulated ±12V output and the isolation between the floating sensing-circuit ground and the power-supply ground. This is critical to operation of the design. The LM317 (U5/LM317/SOT-223 - top right, pg 3) steps the NTA0512's +12V output down to a regulated +5V while the LM337 (U6/LM337/SOT-223 - bottom right, pg 3) steps the NTA0512's -12V output up to a regulated -5V. (A regulated DC-DC-Converter costs much more than an unregulated DC-DC-Converter plus two Voltage Regulators).

Because we are planning to increase the number of Silicon Strip Detector's to 30, 4 boards with 8 channels (current sensors) each would be sensible, allowing two spare sensors in the case of failure.

Prototype Testing

The prototype has been tested here at KU using a pre-amp shaper board and Silicon Strip Detector. The tests were conducted on table-top and at room temperature in three configurations:

1. Silicon Strip Detector (SSD) alone for baseline readings

2. Silicon Strip Detector (SSD) and Sensor with no power to sensor
3. Silicon Strip Detector (SSD) and Sensor with power to sensor

For all configurations, a bias voltage of 50V was applied.

The results are:

Configuration	Bias Current	RMS Noise on the Bias Supply	Sensor Offset
SSD Alone	.17µA	~3.3mV	---
SSD+Sensor (unpowered)	.18µA	~3.3mV	---
SSD+Sensor (powered)	.18µA	~3.3mV	-mV

The linearity of the voltage output of the sensor with respect to bias current was checked:

Bias Current (µA)	0.00	0.24	0.50	0.75	1.00	1.25	1.50	1.75	2.01	2.26	2.51	2.79	3.03
Output Voltage (mV)	+6.4mV	-77.0	-159.0	-240.5	-322.0	-405.0	-487.0	-570.5	-652.0	-732.5	-815.5	-906.0	-983.0

A linear regression fit of this data (using MS Excel) results in a slope of -326.1mV/µA and intercetpt of 3.5mV with a C^2 of 0.99857354.

Sensor response to temperature has been very crudely measured, and seems not to be terribly dependent on ambient temperature. The temperature dependence test was performed by putting a 40MΩ resistor on the Silicon Strip Detector side of the sense resistor, supplying a 50V bias voltage to the power supply side of the sense resistor, placing a 100W light bulb approximately ~10cm above the sensor, and a Hg thermometer ~1cm above the sensor so that the light heated both the board and the thermometer at approximately the same rate. The RMS value of the output voltage was measured with a digital oscilloscope and is as follows:

Temp (°C)	26 (78°F)	29	31	33	35	37	39	41	43	45	47	49	51	53	55 (131°F)
Output (mV)	-405.0	-405.0	-405.0	-405.0	-405.0	-405.0	-406.0	-405.5	-406.0	-406.5	-407.0	-408.0	-408.5	-410.0	-412.0

These data yield a very rough estimate for the slope of the output voltage dependence on temperature of ~-.25mV/1°C= (-412.0mV--405mV)/(55°C-26°C). Because of the .33V/µA factor of gain in the output voltage over input voltage across the 10kΩ sense resistor, this translates to a dependence of the measurement of the bias current on temperature of ~.75nA/°C.

The Cost

The cost of these sensors is broken down:

Components for 30 channels:	$1.5K-$1.6
30 PCB fabricated by APCircuits:	$150-$200
Board population and testing at EDL:	$1K-$1.1K
Total:	$2.65K-$2.9K

These estimates (especially fabrication and population) are for 30 separate channels; costs will almost certainly be reduced somewhat if the final design is for 4 boards of 30 channels each.

Not included in the cost estimate is additional cables - required would be:

1. 1 SMA cable per channel
   The SMA cable currently connecting power supply to pre-amp shaper board could be used to connect sensor to power *or* sensor to pre-amp.
2. Readout cable
   Number and type depend on final configuration.
3. 1 Power per channel
   Because each channel requires a "floating ground", power must be brought in separately for each channel.

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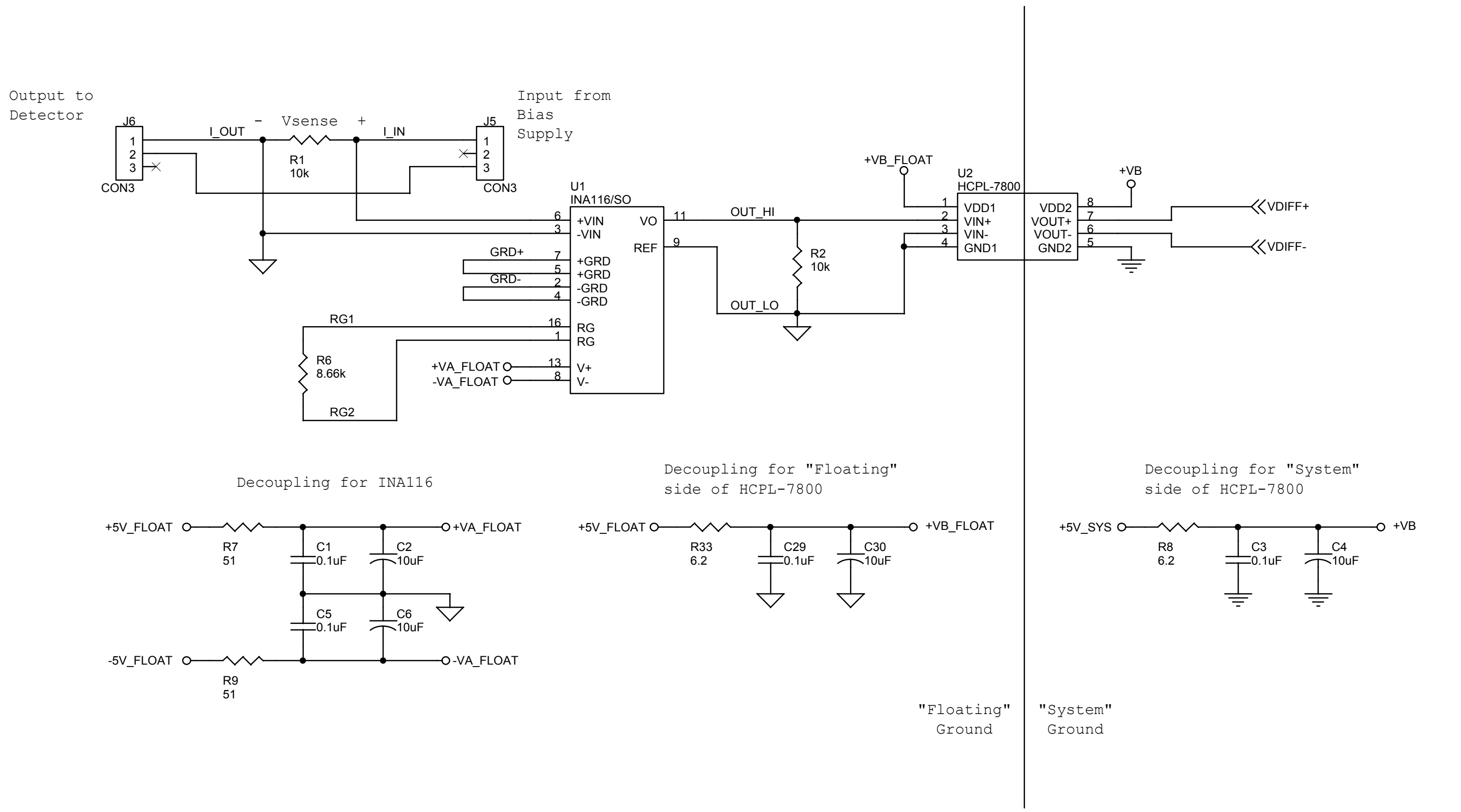

Electronics Design Laboratory

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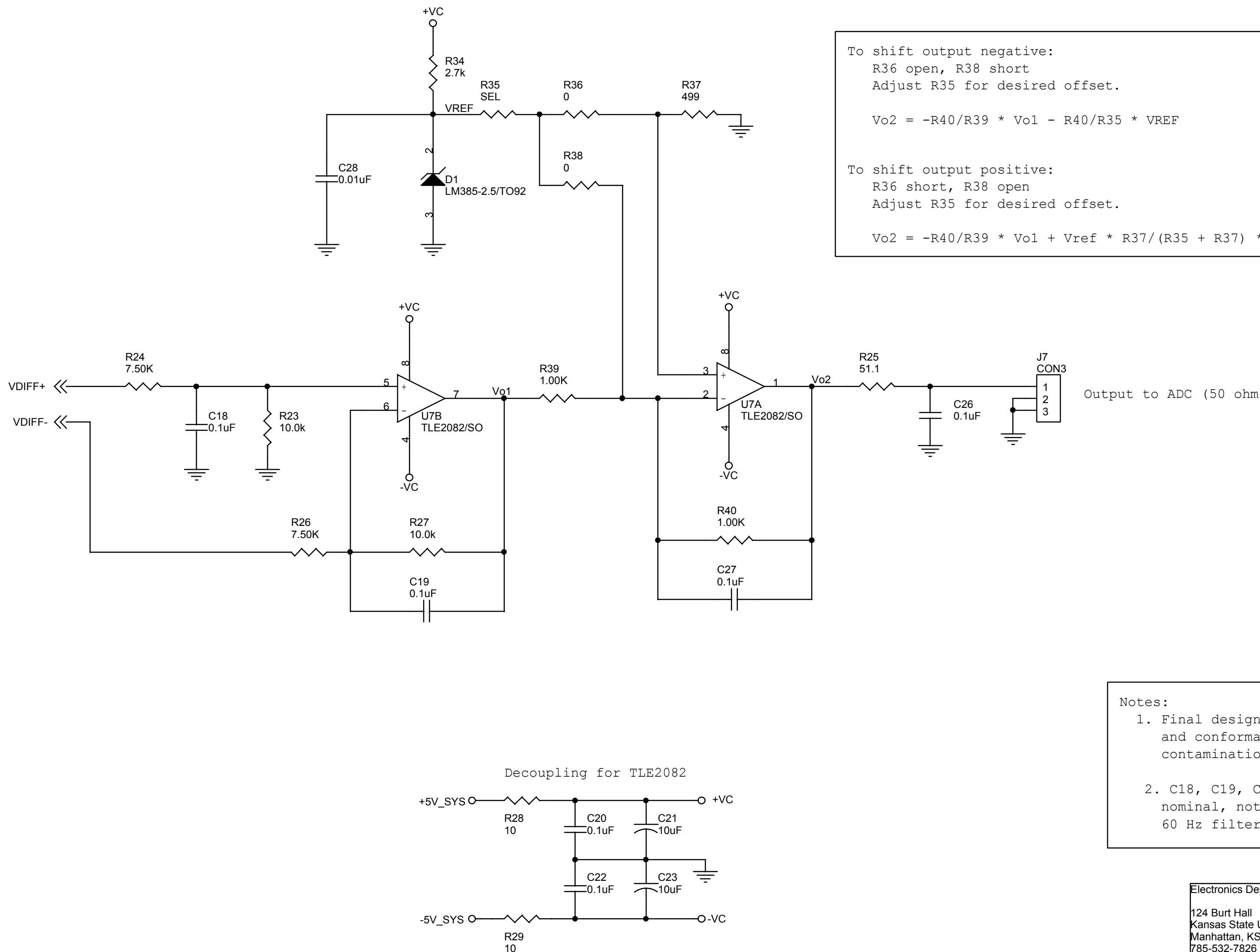
785-532-7826

Title	Floating Instrumentation Amplifier, Isolation Amplifier		
Size B	Document Number BRAHMS Silicon Strip Detector Bias Current Sensor (KUP001)		Rev 4.0
Date:	Thursday, March 15, 2001	Sheet 1 of 3	



To shift output negative:
R36 open, R38 short
Adjust R35 for desired offset.

Vo2 = -R40/R39 * Vo1 - R40/R35 * VREF

To shift output positive:
R36 short, R38 open
Adjust R35 for desired offset.

Vo2 = -R40/R39 * Vo1 + Vref * R37/(R35 + R37) * (1+ R40/R39)

Notes:
1. Final design will require high quality cleaning and conformal coating to prevent surface contamination and leakage.

2. C18, C19, C26 and C27 can be increased (1uF nominal, not polarized) to provide additional 60 Hz filtering.

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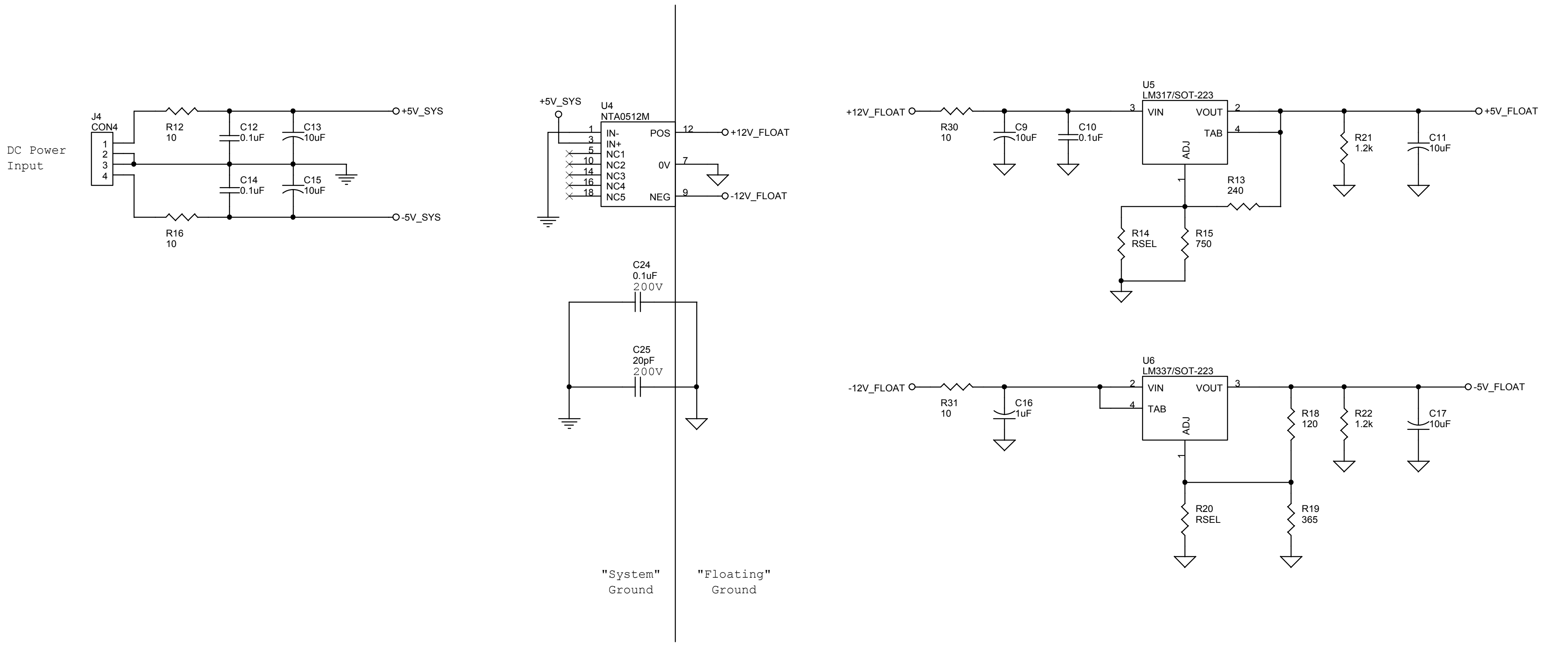
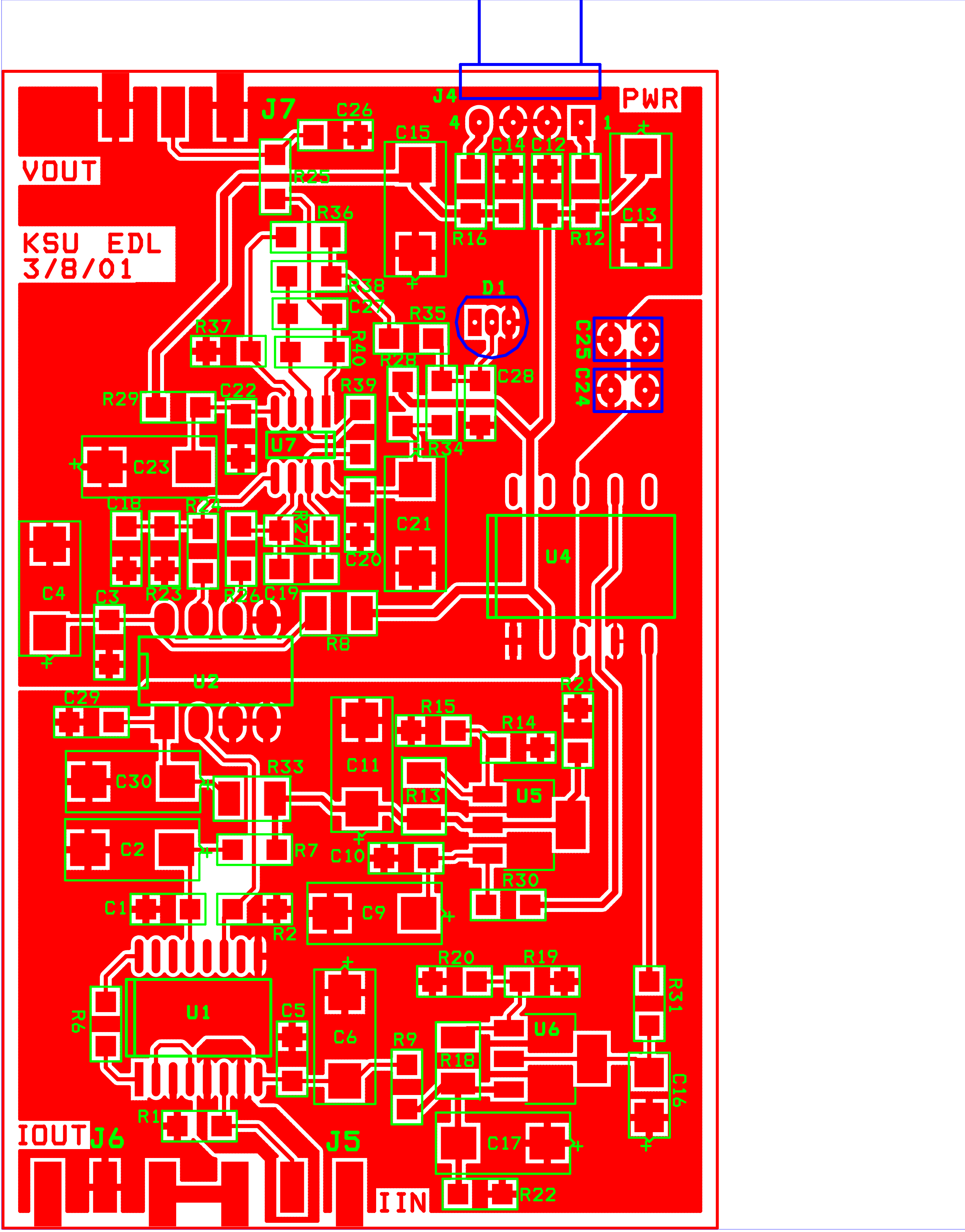
Title	Difference Amplifier, Offset Correction, and Output Driver	
Size B	Document Number BRAHMS Silicon Strip Detector Bias Current Sensor (KUP001)	Rev 4.0
Date:	Thursday, March 15, 2001	Sheet 2 of 3



Electronics Design Laboratory 124 Burt Hall Kansas State University Manhattan, KS 66506 785-532-7826		
Title	Power Input, Isolated Power Generation	
Size B	Document Number BRAHMS Silicon Strip Detector Bias Current Sensor (KUP001)	Rev 4.0
Date:	Thursday, March 15, 2001	Sheet 3 of 3



KU CURRENT SENSOR REV 4.GTD, 10:40 AM, 03/15/01, OrCAD GerbTool